AP/2141

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Dated: 9/21/07 Signature: Joanne Ryan
(Joanne Ryan)

Docket No.: BBNT-P01-128
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Milliken et al.

Application No.: 09/938,921 Confirmation No.: 3501

Filed: August 24, 2001 Art Unit: 2141

For: TERNARY CONTENT ADDRESSABLE MEMORY EMBEDDED IN A CENTRAL PROCESSING UNIT Examiner: Q. N. Nguyen

REPLY BRIEF UNDER 37 C.F.R. 41.41

MS Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

This Reply Brief is submitted in response to the Examiner's Answer, dated July 30, 2007 and re-mailed on September 10, 2007.

I. STATUS OF CLAIMS

Claims 1-16 and 18-21 are pending in this application. Claim 17 was previously canceled without prejudice or disclaimer.

Claims 1-16 and 18-21 were rejected in the Office Action, dated October 5, 2006, and are the subject of the present appeal. These claims are reproduced in the Claim Appendix of the Appeal Brief, filed April 2, 2007.

II. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claim 21 stands rejected under 35 U.S.C. § 101 as directed to non-statutory subject matter.

B. Claims 1-6, 8-15, and 20 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Curtis et al. (U.S. Patent No. 6,000,016) in view of Nataraj et al. (U.S. Patent No. 6,757,779).

C. Claims 7, 16, 18, and 19 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Curtis et al. in view of Nataraj et al., and further in view of Zuraski, Jr. et al. (U.S. Patent No. 6,560,740).

D. Claim 21 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Zuraski, Jr. et al. in view of Nataraj et al.

III. ARGUMENTS

A. GROUNDS OF REJECTION SECTION OF EXAMINER'S ANSWER

In the "Grounds of Rejection" section of the Examiner's Answer (pp. 4-19), the Examiner appears to introduce a new ground of rejection with respect to claim 20. The Examiner appears to reject claim 20 under 35 U.S.C. § 103(a) based on Curtis et al. in view of Nataraj et al. (see Examiner's Answer, p. 5). However, the Examiner relies solely on Nataraj et al. for rejecting all of the features recited in claim 20 and provides no motivation as to why one skilled in the art at the time of Appellants' invention would have realistically been motivated to incorporate the features of claim 20 into the Curtis et al. system (see Examiner's Answer, p. 16). Thus, the Examiner appears to allege for the first time in the Examiner's Answer that Nataraj et al. anticipates claim 20. Appellants object to the Examiner introducing this new ground of rejection for the first time in the Examiner's Answer, particularly since the Examiner has had plenty of opportunities to change this ground of rejection in the six consecutive non-final Office Actions issued by the Examiner prior to the present appeal. Nevertheless, the following remarks address the new rejection of claim 20 in the Examiner's Answer.

1. Claim 20.

Independent claim 20 is directed to a system for forwarding packets in a network device. The system includes means for receiving at least one packet and means for processing the packet using a ternary content addressable memory resident within a central processing unit of the network device. Nataraj et al. does not disclose or suggest this combination of features.

For example, Nataraj et al. does not disclose or suggest means for processing the packet using a ternary content addressable memory resident within a central processing unit of the network

device. The Examiner relies on col. 7, line 38 to col. 9, line 63, of Nataraj et al. for allegedly disclosing this feature (Examiner's Answer, p. 16). Appellants respectfully disagree with the Examiner's interpretation of Nataraj et al.

At col. 7, line 38 to col. 9, line 63, Nataraj et al. discloses information relating to Nataraj et al.'s ternary CAM array 404. Nataraj et al. discloses that ternary CAM array 404 is part of a classification system 400 of a policy-based router (see, for example, Fig. 4; col. 7, lines 38-49). Nataraj et al. in no way discloses or suggests, however, that ternary CAM array 404 is resident within a central processing unit of a network device, as recited in claim 20. Nataraj et al. does not disclose or suggest that classification system 400 is a central processing unit or included within a central processing unit. Thus, this section of Nataraj et al. does not disclose or suggest means for processing a received packet using a ternary content addressable memory resident within a central processing unit of the network device, as recited in claim 20.

For at least the foregoing reasons, Appellants submit that the rejection of claim 20 under 35 U.S.C. § 102(e) based on Nataraj et al. is improper. Moreover, for at least the reasons given in the Appeal Brief, filed April 2, 2007, Appellants submit that the rejection of claim 20 under 35 U.S.C. § 103(a) based on Curtis et al. and Nataraj et al. is improper. Accordingly, Appellants request that the rejection of claim 20 be reversed.

B. RESPONSE TO ARGUMENTS SECTION OF EXAMINER'S ANSWER

In the "Response to Arguments" section of the Examiner's Answer (pp. 19-31), the Examiner merely reiterates many of the allegations that are presented in the "Grounds of Rejection" section of

the Examiner's Answer. Thus, Appellants' arguments presented in the Appeal Brief, filed April 2, 2007, are applicable to those allegations. Appellants submit the following additional remarks.

Rejection under 35 U.S.C. § 101

In section A of the "Response to Arguments" section of the Examiner's Answer, the Examiner admits that Appellants' claim 21 falls under one of the enumerated categories of patentable subject matter recited in 35 U.S.C. § 101 (Examiner's Answer, p. 20). The Examiner then alleges:

> To satisfy section 35 USC § 101 requirements (*i.e., to satisfy the condition of a* ***new and useful machine)***, the claim must be for a practical application of a 35 USC § 101 judicial exception

(emphasis in original) (Examiner's Answer, p. 20). Appellants disagree.

It is well established that the judicial exceptions under 35 U.S.C. § 101 for patentable subject matter include laws of nature, natural phenomena, and abstract ideas. See, for example, Diamond v. Diehr, 450 U.S. 175, 185, 209 USPQ 1, 7 (1981). The invention recited in claim 21 is not a law of nature, a natural phenomena, or an abstract idea and, thus, does not fall under one of the judicial exceptions of 35 U.S.C. § 101.

Further, the Examiner has not provided any evidence that claim 21, which is directed to an arithmetic logic unit that includes a register unit; an operations unit; and a ternary content addressable memory coupled to the register unit and the operations unit within the arithmetic logic unit, falls under one of the judicial exceptions of 35 U.S.C. § 101 or to a practical application of a 35 U.S.C. § 101 judicial exception. Accordingly, the Examiner has not established a *prima facie* basis for denying patentability under 35 U.S.C. § 101.

The Examiner further alleges:

> Specially, it does not appear to produce a tangible result because merely describing *"a ternary content addressable memory coupled to a register unit and an operations unit within an arithmetic logic unit"* fails to describe, to use, or to make available for use, the result of the description in order to enable its functionality and usefulness to be realized, i.e., **fails to describe a "new and useful machine"**

(emphasis in original) (Examiner's Answer, p. 20). Appellants disagree.

As set forth above, the invention recited in claim 21 falls under one of the enumerated categories of patentable subject matter under 35 U.S.C. § 101 and does not fall under one of the judicial exceptions of 35 U.S.C. § 101. Accordingly, claim 21 is directed to statutory subject matter under 35 U.S.C. § 101.

For at least the foregoing reasons and for at least those reasons given in the Appeal Brief, filed April 2, 2007, Appellants request that the rejection of claim 21 under 35 U.S.C. § 101 as directed to non-statutory subject matter be reversed.

Rejection under 35 U.S.C. § 103(a) based on Curtis et al., Nataraj et a.l, and Zuraski, Jr. et al.

In section I of the "Response to Arguments" section of the Examiner's Answer, the Examiner alleges:

> In response to the Appellant's additional argument that ***"Zuraski, Jr. et al. does not disclose or suggest that repair logic unit 70 is an arithmetic logic unit"*** (as recited in page 22 of the Appeal Brief), Examiner respectfully submits that one of ordinary skill in the art at the time of the invention would have duly recognized that **Zuraski's** disclosed mechanism for comparing provided address signals with the contents of memory locations would require the use of a content addressable memory CAM 82 located within a repair logic unit 70 in order to perform the matching operations as intended **(Zuraski, Fig. 8 and col. 9, line 47 – col. 10, line 5)**. In absence of any disclosure by the Appellant of specifically why using an arithmetic logic unit provides any sort of an advantage, is used for a particular purpose, or solves a specific problem, consequently, one of ordinary skill in the art would have readily found that it is obvious to incorporate the feature of locating/embedding the content addressable memory within the logic unit as disclosed by **Zuraski**, into the teachings

> of **Curtis-Nataraj** to achieve the claimed invention as recited in claim 7 and claim 16

(emphasis in original) (Examiner's Answer, pp. 29-30). Appellants strenuously object to the Examiner's impermissible attempt to shift the burden to Appellants to explain why the recited arithmetic logic unit provides an advantage over Zuraski, Jr. et al.'s repair logic unit 70, is used for a particular purpose, or solves a specific problem. The fact remains that the Examiner has not explained why one skilled in the art at the time of Appellants' invention would have reasonably construed Zuraski, Jr. et al.'s repair logic unit 70 as an arithmetic logic unit, as that device is commonly known in the art. Appellants have repeatedly explained to the Examiner that an "arithmetic logic unit" is a specific kind of device (typically one with two inputs, a function select input, and one output containing the result of the function applied to the two inputs). A common example of an arithmetic logic unit is the TTL 74181 arithmetic logic unit chip and its various descendants. Either the Examiner does not appreciate what an arithmetic logic unit is or chooses to ignore the known meaning of this device. In either case, the Examiner has not established a *prima facie* case of obviousness with respect to claims 7 and 16.

For at least these additional reasons and for at least those reasons given in Appellants' Appeal Brief, filed April 2, 2007, Appellants respectfully request that the rejection of claims 7 and 16 based on Curtis et al., Nataraj et al., and Zuraski, Jr. et al. be reversed.

IV. CONCLUSION

In view of the foregoing arguments, Appellants respectfully solicit the Honorable Board to reverse the Examiner's rejection of claims 1-16 and 18-21 under 35 U.S.C. §§ 101 and 103.

Appellants believe no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 18-1945, under Order No. BBNT-P01-128 from which the undersigned is authorized to draw.

Dated: September 21, 2007

Respectfully submitted,

By _____

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